AMENDMENTS TO THE CLAIMS:

Please amend claim 1 as indicated below. This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a first wiring formed above said semiconductor substrate with a first insulating film interposed therebetween;

an MIM capacitor formed above said first insulating film;

a second insulating film formed to cover an upper electrode of said MIM capacitor;

a second wiring formed on said second insulating film; and

a guard ring buried in said second insulating film surrounding said MIM capacitor;

wherein said guard ring is provided such that said guard ring is electrically insulated from said first wiring, said second wiring, and said MIM capacitor.

2. (Original) The semiconductor device according to claim 1, wherein

said second wiring is connected to said first wiring via a hole formed in said second insulating film.

3. (Original) The semiconductor device according to claim 2, wherein

said guard ring is a metal ring formed of the same material as said second wiring, said metal ring being buried in said second insulating film so as to penetrate through said second insulating film.

4. (Original) The semiconductor device according to claim 3, wherein said metal ring is in an electrically floating state.

5. (Previously Presented) The semiconductor device according to claim 3, wherein said second wiring and metal ring are formed of copper layers with barrier metals formed thereunder.

6. (Original) The semiconductor device according to claim 1, wherein the relative dielectric constant of said second insulating film is equal to 3.5 or less.

7. (Original) The semiconductor device according to claim 6, wherein said second insulating film is a fluorine containing silicon oxide film.

8. (Original) The semiconductor device according to claim 6, wherein said second insulating film is a carbon containing silicon oxide film.

9. (Original) The semiconductor device according to claim 6, wherein said second insulating film is a porous silicon oxide film.

10. (Original) The semiconductor device according to claim 1, wherein

said guard ring is so disposed as to cut a seam generated in said second insulating film around said MIM capacitor.

11. (Original) The semiconductor device according to claim 1, wherein

a width of said guard ring is in a range of 0.1 to 1 μm.

12. (Original) The semiconductor device according to claim 1, further comprising:

a block insulating film formed between said first and second insulating film to cover said first wiring.

13. (Original) The semiconductor device according to claim 1 further comprising:

contact plugs formed of the same material as said second wiring and buried in said second insulating film to be contacted to bottom and top electrodes of said MIM capacitor;

a third insulating film formed over said second insulating film to cover said second wiring; and

a third wiring formed on said third insulating film to electrically connect at least one of said first and second wirings to said MIM capacitor.

14. (Original) The semiconductor device according to claim 13, wherein

said third wiring is coupled to said MIM capacitor via said contact plugs.

15. (Withdrawn) A method of fabricating a semiconductor device comprising:

forming a first wiring above a semiconductor substrate with a first insulating film interposed therebetween;

forming an MIM capacitor above said first insulating film;

forming a second insulating film to cover said MIM capacitor; and

burying a second wiring in the surface of said second insulating film, and a guard ring in said second insulating film to surround said MIM capacitor.

16. (Withdrawn) The method according to claim 11, wherein

said second wiring and guard ring are simultaneously formed by forming via hole, wiring groove continued from said via hole and guard ring groove surrounding said MIM capacitor; and burying wiring material in said via hole, wiring groove and guard ring groove.

17. (Withdrawn) The method according to claim 11, further comprising:

forming a third insulating film over said second insulating film to cover said second wiring; and

burying a third wiring by a dual damascene process in the surface of said third insulating film to electrically connect at least one of said first and second wirings to said MIM capacitor.

18. (Withdrawn) The method according to claim 15, wherein

said second wiring and metal ring are formed of cupper layers with barrier metals formed thereunder.

19. (Withdrawn) The method according to claim 15, wherein

the relative dielectric constant of said second insulating film is equal to 3.5 or less.

20. (Withdrawn) The method according to claim 15, wherein

said guard ring is so disposed as to cut a seam generated in said second insulating film around said MIM capacitor.